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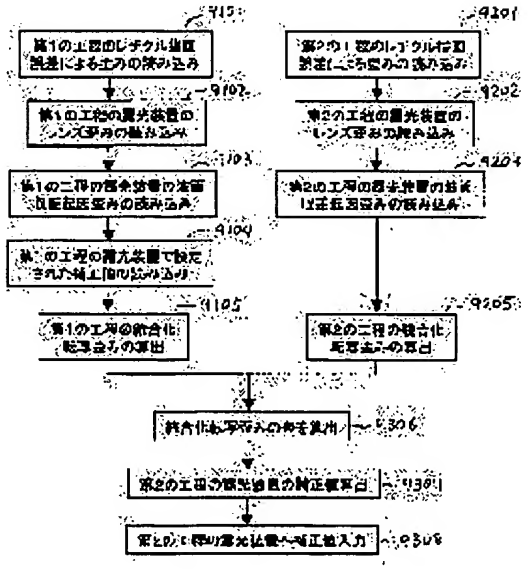
(54) METHOD AND SYSTEM FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To solve the problem of an advanced shrinkage device that a single aligner is used from the first step to the last step in order to avoid misalignment due to the difference of strain between exposing lenses but lowering in the availability of an expensive aligner due to the increase of work-in-process and the occurrence of waiting time blocks cost reduction.

SOLUTION: In the method for manufacturing a semiconductor device, strain of lens, coma and writing error of reticle are measured previously, the combination of an aligner and their correction values satisfying the regulation of the relevant process/product is calculated dynamically from shot size, device pattern and illumination conditions and then work using an aligner satisfying the regulation is designated.

図1



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CLAIMS

[Claim(s)]
[Claim 1] In the 1st exposure process, expose a substrate by the 1st circuit pattern, and the 1st circuit pattern is formed on this substrate. It is the manufacture approach of the semiconductor device which forms the 2nd circuit pattern which exposes said substrate which formed said 1st circuit pattern in the 2nd exposure process by the 2nd circuit pattern, and is electrically connected to said 1st circuit pattern. It asks for the comprehensive imprint-ized distortion of the 1st when exposing said substrate by the 1st circuit pattern in said 1st exposure process. It asks for the comprehensive imprint-ized distortion of the 2nd when exposing said substrate by the 2nd circuit pattern in said 2nd exposure process. The correction value of the 2nd exposure process is calculated based on said comprehensive imprint-ized distortion of the 1st, and said comprehensive imprint-ized distortion of the 2nd. The manufacture approach of the semiconductor device characterized by exposing the 2nd circuit pattern and forming the 2nd circuit pattern on the 1st [said] circuit pattern formed through said 1st exposure process in the 2nd exposure process amended with this correction value
[Claim 2] Said comprehensive imprint-ized distortion of the 1st is the manufacture approach of the semiconductor device according to claim 1 characterized by being two-dimensional distortion which unified a reticle drawing error [in / it is two-dimensional distortion which unified the reticle drawing error in said 1st exposure process, and lens distortion and distortion of a wave aberration reason, and / in said comprehensive imprint-ized distortion of the 2nd / said 2nd exposure process], and lens distortion and distortion of a wave aberration reason.
[Claim 3] The process which is the manufacture approach of a semiconductor device and applies the 1st resist to a substrate front face, The 1st exposure process which carries out the exposure imprint of the 1st circuit pattern at the 1st resist applied on said substrate using the 1st aligner,

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the manufacture approach of the semiconductor device which makes it possible to reduce generating of the doubling gap with a lower layer pattern in an exposure process, and to expose the upper pattern about the manufacture approach of a semiconductor device, and its system.
[0002]
[Description of the Prior Art] Manufacture of a semiconductor device is performed by etching the film by repeating the process of generating a circuit pattern on a semi-conductor wafer, on each class, after forming the electric conduction film or an insulator layer on a semi-conductor wafer, exposing to a resist the resist which is a sensitization agent and developing the circuit pattern on spreading and reticle on this. At this time, to a substrate layer pattern, if there is a location gap of the circuit pattern at the time of exposure, a circuit will disconnect or short-circuit and will serve as a defect of a semiconductor device. For this reason, an aligner detects optically the alignment mark which is in the periphery of a circuit pattern in advance of exposure of a circuit pattern, and is performing alignment of a substrate layer and an exposure layer by amending measurement and an imprint location for the location of a substrate layer. Since distortion of a projection lens differs between equipment when an aligner which is different in a substrate layer and an exposure layer is used at this time, even if it performs alignment in an alignment mark location, it doubles in the circuit pattern section and a gap arises. For this reason, at the exposure process, the commencement-of-work method (No. limited commencement of work) using the same aligner is always adopted from the first process to the final process.
[0003] However, this is a big cause which the operating ratio of an expensive aligner does not go up, and some policies for utilizing two or more aligners between processes are indicated. For example, there is the approach of amending the lens distortion between 2 equipment for a scale factor as indicated by the publication-number No. 92609 [nine to] official report. Moreover, the approach of judging from the difference of the lens distortion between 2 equipments is indicated [whether construction work can be started in a provisional-publication-of-a-patent No. 114132 / 2000 to / official report with Aligner B to the wafer which started construction work with Aligner A, and]. Moreover, the approach of amending the drawing error of reticle by the scale factor of an aligner, a revolution, and perpendicularity control of the stage at the time of scan exposure is indicated by the provisional-publication-of-a-patent No. 124125 [2000 to] official report.
[0004]
[Problem(s) to be Solved by the Invention] There are the following troubles about the above-mentioned well-known technique. That is, the consideration to wave optics-distortion has fallen out in the above-mentioned example. About lens distortion, there are geometrical optics-distortion and wave optics-distortion of aberration reasons of a lens, such as comatic aberration. Drawing 11 explains the latter.
[0005] The exposure lens 30 has comatic aberration 300 as wave aberration. This is the unsymmetrical aberration resulting from the profile irregularity error of the eccentricity of the element lens for example, at the time of exposure lens 30 assembly, a tilt, and a lens side. on the occasion of exposure, it is shown in drawing 11 (a) -- usually -- everything but lighting -- "-- the number for optical alliance January, 1998 -- zona-orbicularis lighting which is indicated by 4th page" may be applied Exposure with zona-orbicularis lighting is shown in drawing 11 (b). With zona-orbicularis lighting, the cross section of the illumination-light bundle 2002 is the zona orbicularis-like, and it is effective in raising the contrast of an imprint pattern.
[0006] Comatic aberration 300 is as large as the circumference of the exposure lens 30. Therefore, imprint pattern location gap deltaX' of the zona-orbicularis lighting with which the flux of light spreads on the outskirts as shown in drawing 11 usually becomes larger than location gap deltaX in lighting. That is, a location gap of an imprint pattern

changes according to the intensity distribution of the flux of light which passes along the exposure lens 30. Moreover, since the locations of the diffracted light which passes along the inside of the exposure lens 30 with the spatial frequency of an imprint pattern but where an illumination-light bundle is the same differ, the amounts of location gaps differ. Drawing 12 shows the case where the exposure light 2003 carries out incidence to a coarse pattern 210 and the coarse detailed pattern 220. Since it passes along the circumference of the exposure lens 30 compared with the case where the direction of the diffracted light 2005 of the detailed pattern 220 with the large angle of diffraction of (b) is the coarse pattern 210 of (a), it becomes larger than amount of location gaps deltax' of (b) rather than amount of location gaps deltax' of (a).

[0007] In order for a location gap of wave optics-distortion, i.e., a wave aberration reason, to change with lighting conditions and imprint pattern sizes from the above thing, it is necessary to compute the magnitude of wave aberration, and lighting conditions and imprint pattern size as a parameter.

[0008] Moreover, according to the direction [each point / image surface top] of distortion, lens distortion which is an above-mentioned wave optics-distortion and geometrical optics-distortion, and the distortion by the reticle drawing error increase at a certain point, and are reduced at a certain point. Therefore, the distortion of the imprint image obtained these results is obtained by adding each distortion two-dimensional. Only one of three distortion is taken into consideration, or the concept [distortion / by two-dimensional addition / integrative] of handling has escaped from the above-mentioned well-known example.

[0009] The object of this invention is giving the manufacture approach of a semiconductor device of performing number machine limited relaxation of an aligner by performing amendment in consideration of an integrative two-dimensional distortion which consists of the above-mentioned geometric lens distortion, wave optics-distortion of a wave aberration reason, and distortion by the reticle drawing error. The new description of this invention will become clear from description and the accompanying drawing of this description.

[0010]

[Means for Solving the Problem] In order to attain the above-mentioned object, in this invention, in the 1st exposure process, expose a substrate by the 1st circuit pattern, and the 1st circuit pattern is formed on this substrate. In the manufacture approach of the semiconductor device which forms the 2nd circuit pattern which exposes the substrate which formed the 1st circuit pattern in the 2nd exposure process by the 2nd circuit pattern, and is electrically connected to the 1st circuit pattern It asks for the comprehensive imprint-ized distortion of the 1st when exposing a substrate by the 1st circuit pattern in the 1st exposure process. It asks for the comprehensive imprint-ized distortion of the 2nd when exposing a substrate by the 2nd circuit pattern in the 2nd exposure process. The correction value of the 2nd exposure process is calculated based on the comprehensive imprint-ized distortion of the 1st, and the comprehensive imprint-ized distortion of the 2nd. On the 1st circuit pattern formed through the 1st exposure process in the 2nd exposure process amended with this correction value, the 2nd circuit pattern is exposed and the 2nd circuit pattern was formed.

[0011] In order to attain the above-mentioned object, moreover, in this invention The process which applies the 1st resist to a substrate front face in the manufacture approach of a semiconductor device, The 1st exposure process which carries out the exposure imprint of the 1st circuit pattern at the 1st resist applied on the substrate using the 1st aligner, The process which carries out etching processing of the substrate which carried out the exposure imprint of this 1st circuit pattern, and forms the 1st circuit pattern, The process which forms an insulator layer in the substrate in which the 1st circuit pattern was formed, and the process which applies the 2nd resist on a substrate, The 2nd exposure process which carries out the exposure imprint of the 2nd circuit pattern at the 2nd resist applied on the substrate using the 2nd aligner, It sets at the 2nd exposure process including the process which carries out etching processing of the substrate which carried out the exposure imprint of the 2nd circuit pattern, and forms the 2nd circuit pattern. Where amendment based on a reticle drawing error and lens distortion of as opposed to the 1st aligner for the 2nd aligner, and distortion of a wave aberration reason is performed, the 2nd circuit pattern was exposed.

[0012] In order to attain the above-mentioned object, moreover, in this invention In the manufacture approach of the semiconductor device which exposes the circuit pattern of the 2nd process on the circuit pattern of the 1st process (1) The step which reads distortion by the reticle drawing error of said 1st process, (2) The step which reads the lens distortion in the aligner of said 1st process, (3) The step which reads the wave aberration reason distortion in the aligner of said 1st process, (4) The step which reads the correction value set up with the aligner of said 1st process, (5) -- the step which computes distortion by which said 1st process was integrated, and (6) -- with the step which reads distortion by the reticle drawing error of said 2nd process (7) The step which reads the lens distortion in the aligner of said 2nd process, (8) The step which reads the wave aberration reason distortion in the aligner of said 2nd process, (9) -- the step which computes the integration imprint distortion of said 2nd process, and (10) -- with the step which computes that of the difference of the integration imprint distortion of said 2nd process, and the integration imprint distortion of said 1st

process (11) It is characterized by having the step which computes the correction value in the aligner of said 2nd process which makes said difference min.

[0013] Since the difference of a near imprint distortion is actually computable by this between two aligners which unified a reticle drawing error, lens distortion, and distortion of a wave aberration reason, it becomes possible to compute correction value with a high precision in the 2nd aligner.

[0014] moreover -- as the manufacture approach of a semiconductor device into which the above was developed -- (12) -- with the step which searches the identifier of reticle and the identifier of an aligner which were used at said 1st process (13) The step which reads distortion by the drawing error of the reticle used at said 1st process, (14) The step which reads the lens distortion in the aligner used at said 1st process, (15) The step which reads the wave aberration reason distortion in the aligner used at said 1st process, (16) The step which reads the correction value at the time of exposure of the aligner used at said 1st process, (17) The step which computes the imprint distortion by the 1st process from the data of (16) from said step (12), (18) The step which reads distortion by the drawing error of the reticle in said 2nd process, (19) The step which reads the lens distortion of an aligner candidate in said 2nd process, (20) The step which reads the wave aberration reason distortion of an aligner candidate in said 2nd process, (21) The step which computes the integration imprint distortion by the 2nd process from the data of said step (18), (19), and (20), (22) The step which computes the difference of integration imprint distortion in the integration imprint distortion and said 2nd process in said 1st process, (23) -- the location gap after the correction value which makes difference of said integration imprint distortion min, and amendment -- with the step which computes the maximum of difference The maximum of difference is compared with the value of standard set up beforehand. (24) -- the location gap after said amendment -- When smaller than a value of standard, they are recorded or outputted, using said aligner candidate and said correction value as data, and when larger than a value of standard, it is characterized by having the step which chooses the aligner candidate according to return as a step (19).

[0015] Since this becomes possible in the 2nd process to choose the equipment which is vacant out of two or more aligners with which are satisfied of the specification of doubling, an equipment operating ratio can be raised.

[0016] Furthermore, the step which reads distortion of the wave aberration reason of the aligner in the 1st process and 2nd process (25) The step which reads the lighting conditions of this aligner, and the step which reads the dimension information on the circuit pattern on (26) reticles, (27) -- the step which reads the wave aberration for every image quantity of this aligner, and (28) -- with said lighting conditions, said dimension information, and the step that computes the image of said circuit pattern from the wave aberration for said every image quantity (29) It is characterized by having the step which computes distortion of a wave aberration reason from a location gap of the image of said circuit pattern.

[0017] Since this computes wave aberration reason distortion not as a fixed value but as a value depending on lighting conditions and a circuit pattern dimension, the data of the wave aberration reason distortion near a more nearly actual value can be obtained.

[0018] and in the manufacture approach of the above-mentioned semiconductor device, step (13) - (23) and step (25) - (29) carries out about a specific aligner, reticle, lighting conditions, and a circuit pattern dimension -- having -- every combination of specific conditions -- the location gap after correction value and amendment -- the value of difference is computed beforehand and stored in the storage.

[0019] thereby -- the location gap after correction value and amendment -- since the calculation time amount of the value of difference is omissible, it becomes possible to acquire the combination of the aligner which fulfills doubling specification, and corresponding correction value at a high speed.

[0020] In order to attain the above-mentioned object, moreover, in this invention A history storage means to memorize the aligner and the lighting conditions of having used for manufacture of an exposed substrate the semiconductor device manufacturing system which exposes the circuit pattern of the 2nd process on the circuit pattern of the 1st process, correction value, and the history of reticle, A reticle data storage means to memorize the drawing error reason distortion for every reticle, and a typical circuit pattern dimension, A lens distortion storage means to memorize the lens distortion for every aligner, and a wave aberration data storage means to memorize every aligner and the wave aberration data for every image quantity, A wave aberration reason distortion calculation means to compute wave aberration reason distortion from the wave aberration for every said lighting condition, said circuit pattern dimension, and said image quantity, A wave aberration reason distortion storage means to memorize said wave aberration reason distortion, and an integration imprint distortion calculation means to compute integration imprint distortion from said reticle data, said lens distortion data, and said wave aberration data, the difference of two integration imprint distortion -- computing -- this -- with a correction value calculation means to compute the correction value which makes difference min A combination information storage means to memorize a doubling specification storage means to memorize a product and

the doubling specification for every process, said two aligners, said lighting conditions, the information on said reticle, corresponding correction value, and integration imprint distortion maximum, The history information about the 1st process corresponding to said exposed substrate is read from a history storage means. The aligner of this history information, lighting conditions, the aligner of the 2nd process corresponding to reticle, By comparing the difference of said integration imprint distortion corresponding to lighting conditions, and the doubling specification and the 1st process corresponding to the 2nd process for a candidate, and the 2nd process of reticle A commencement-of-work decision means to have compared with the system operating status of a actual aligner the aligner which can start construction work, lighting conditions, a candidate selection means to choose the candidate of reticle, and the candidate of the aligner, in which said commencement of work is possible, and to judge the aligner which starts construction work was had and constituted.

[0021] Thereby, acquisition of the correction value between 2 equipments by integration imprint distortion and selection of the aligner in consideration of doubling specification which can be started can carry out efficiently.

[0022]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing. A processing flow for drawing 1 to compute the correction value of the aligner in the semiconductor device production process which is 1 operation gestalt of this invention, and drawing 2 show the mimetic diagram of the target two-dimensional-in processing flow distortion data. First, the processing flow for computing the correction value of an aligner by drawing 1 is explained.

[0023] First, the distortion data based on the drawing error of the reticle in the 1st process are read at step 9101. Next, the lens distortion data of the aligner in the 1st process are read at step 9102. Furthermore, the distortion data of a wave aberration reason of the aligner in the 1st process are read at step 9103. Moreover, at step 9104, the correction value set as the aligner of the 1st process is read. Correction value is the scale factor of the reticle scanning direction in the imprint image for example, at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image here. Next, the integration imprint distortion of the 1st process is computed by adding the distortion, lens distortion, and wave aberration reason distortion by the reticle drawing error in the 1st process, and amending this with the above-mentioned correction value by step 9105.

[0024] Next, in steps 9201-9203, the integration imprint distortion of the 2nd process is computed by reading each data of distortion by the reticle error in the 2nd process, lens distortion, and wave aberration reason distortion, and adding these at step 9205.

[0025] Next, by step 9306, the difference of the integration imprint distortion in the 1st and 2nd processes computed at steps 9105 and 9205 is computed, and the correction value of the aligner in the 2nd process for amending difference at step 9307 is computed. This correction value is the scale factor of the reticle scanning direction in the imprint image at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image like the above.

[0026] Finally in step 9308, this correction value is inputted into the aligner of the 2nd process.

[0027] Thus, the resist which carried in to the aligner of the 1st process the semi-conductor wafer which applied the resist to the front face, and was applied to this semi-conductor wafer front face using the 1st mask where correction value is inputted into the aligner of the 2nd process is exposed, and the 1st circuit pattern is imprinted. The 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 1st circuit pattern at the development process, and carried out the exposure imprint of the 1st circuit pattern, and was developed at the etching process after that.

[0028] Then, after forming an insulator layer on the 1st circuit pattern formed in this semi-conductor wafer and applying a resist to a front face, it carries in to the aligner of the 2nd process, and the resist applied to this semi-conductor wafer front face using the 2nd mask is exposed, and the 2nd circuit pattern is imprinted. The 2nd circuit pattern electrically connected to the 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 2nd circuit pattern at the development process, and carried out the exposure imprint of the 2nd circuit pattern, and was developed at the etching process after that.

[0029] Next, drawing 2 explains each distortion data in the processing flow for computing the correction value of the aligner of drawing 1 . The distortion measure point of the distortion data 21 based on the reticle error of the 1st process is the grid 213 which consisted of reticle marks 211 and 212 of right and left used as the criteria of reticle alignment,

and a circuit pattern chosen from the design data. An absolute coordinate is measured by the coordinate measuring device with which these were equipped with the laser length measuring machine etc. The distortion data 21 based on a reticle error consist of what asked for the difference delta Rxi and delta Ryi of the x directions of the coordinate on the design of each circuit pattern obtained when the scale factor of a design-data coordinate and a revolution are amended so that the measurement coordinate of the reticle marks 211 and 212 may be in agreement with the coordinate on a design, and the actually measured coordinate, and the direction of y in each measure point i, and the absolute coordinate itself which measured the reticle marks 211 and 212. The distortion data 22 based on the reticle error of the 2nd process are also obtained in the same procedure as the above.

[0030] The distortion data 31 of the aligner in the 1st process expose the reticle for assessment other than the product reticle of each above-mentioned process in which the pattern arranged on a grid is contained on an exposed substrate, and are obtained by measuring the formed imprint pattern with the above-mentioned coordinate measuring device. Moreover, although the reticle marks 311 and 312 on reticle are not exposed with the gobo (masking blade) of an aligner, they are usually exposed on an exposed substrate to a pattern and coincidence by this measurement, without shading. The coordinate of the reticle marks 311 and 312 formed in the exposed substrate is also measured, and it includes in the distortion data 31 of the aligner in the 1st process. In case [in which this is based on a reticle error later] distortion of an aligner is added distorted, it is used for carrying out alignment of both distorted data.

[0031] Here, how to ask for the distortion data 31 of an aligner from the measurement coordinate of the imprint pattern arranged on the grid of the above-mentioned reticle for assessment is explained. For that, amendment first needs to remove position error deltaSrxi of the x directions of each pattern of a drawing error reason of the reticle for distortion measurement assessment, and the direction of y, and deltaSryi. i corresponds to Pattern i. deltaSrxi and deltaSryi are obtained by "the-one number" and "a-two number."

[0032]

[Equation 1]

$$\Delta Srx_i = Srx_i - Sdx_i \quad \cdots (数1)$$

[0033]

[Equation 2]

$$\Delta Sry_i = Sry_i - Sdy_i \quad \cdots (数2)$$

[0034] The absolute-measurement coordinate of the x directions of each pattern [in / here / in Srxi and Sryi / the reticle for assessment] i and the direction of y, Sdxi, and Sdyi are the design value coordinates of the x directions of each pattern i in the reticle for assessment, and the direction of y. On the other hand, distortion data deltaSlenxi of the aligner in the 1st process and deltaSlenyi are obtained by "the-three number" and "a-four number."

[0035]

[Equation 3]

$$\Delta Slenx_i = Smx_i - Srx_i \quad \cdots (数3)$$

[0036]

[Equation 4]

$$\Delta Sleny_i = Smy_i - Sry_i \quad \cdots (数4)$$

[0037] Smxi and Smyi are the measured value of the absolute coordinate of an imprint pattern [in / here / an exposed substrate]. therefore, "a-one number", "a-two number", "a-three number", and "a-four number" -- deltaSlenxi and deltaSlenyi -- [0038]

[Equation 5]

$$\Delta Slenx_i = Smx_i - Sdx_i + \Delta Srx_i \quad \cdots (数5)$$

[0039]

[Equation 6]

$$\Delta Sleny_i = Smy_i - Sdy_i + \Delta Sry_i \quad \cdots (数6)$$

[0040] It becomes. The distorted data 31 of the aligner in the 1st process are obtained by these actuation. The distorted data 32 of the aligner in the 2nd process are also obtained by same actuation.

[0041] Next, how to ask for the wave aberration reason distortion data 41 of the aligner in the 1st process is explained. The above-mentioned distortion data 31 base [geometrical optics-distortion is shown and] on the magnitude and the

lighting conditions of a pattern and are fixed. However, intensity distribution are in the imprint diffracted light according to the magnitude and the lighting conditions of a pattern in wave optics. Since the weight of the passage location in an exposure lens differs, the deflection from the distorted data 31 of the aligner which is geometrical optics-distortion arises in an imprint location by wave aberration. It is the distortion data 41 of a wave aberration reason which showed this deflection.

[0042] As drawing 5 and drawing 6 were quoted and explained previously, the distortion of a wave aberration reason is dependent on the spatial frequency of wave aberration and lighting conditions, or a pattern. Then, by inputting measurement punishment, this, a reticle pattern, and lighting conditions for the wave aberration 300 for every image quantity of the exposure lens 30 beforehand, it asks for the imprint image on an exposed substrate by wave optics-numerical calculation, and location gap deltaX' is computed. The count approach of an imprint image is 'Y.Yoshitake et al, SPIE Vol.1463, pp 678-679, and 1991'. It is indicated. A location gap is given by computing the difference delta Wxi and delta Wyi of the center of gravity of the optical intensity distribution of an imprint image, and a reticle pattern-design location for example, in each image quantity i of every. Moreover, when asking for integration imprint distortion by the distorted data 31 of an aligner and the addition of the wave aberration reason distortion 41 which are geometrical optics-distortion, in each image quantity, it asks for a location gap as difference of the core of the optical intensity distribution of an imprint image, and the distorted data 31 of an aligner. In addition, the wave aberration reason distortion data 42 of the aligner in the 2nd process are also obtained by same actuation.

[0043] deltaxixi and deltaxiyi which are the integration imprint distortion data 51 are obtained by the degree type.

[0044]

[Equation 7]

$$\Delta\xi x_i = \Delta Srx_i + \Delta Slenx_i + \Delta Wx_i \quad \cdots (数7)$$

[0045]

[Equation 8]

$$\Delta\xi y_i = \Delta Sry_i + \Delta Sleny_i + \Delta Wy_i \quad \cdots (数8)$$

[0046] The aligner is performing shot amendment of the exposure layer to a substrate layer by rotating an exposed substrate. Moreover, in the case of the scanning aligner, control of the stage in which an exposed substrate is carried is performing the scale factor and shot failure component of a scanning direction. Therefore, delta xi'xi and delta xi'yi which are the integration imprint distortion data 53 which considered the shot correction value of the exposure layer to a substrate layer are [0047].

[Equation 9]

$$\Delta\xi' x_i = a(X_i + \Delta\xi x_i) + b(Y_i + \Delta\xi y_i) + \Delta x - X_i \quad \cdots (数9)$$

[0048]

[Equation 10]

$$\Delta\xi' y_i = c(X_i + \Delta\xi x_i) + d(Y_i + \Delta\xi y_i) + \Delta y - Y_i \quad \cdots (数10)$$

[0049] Correction value for a, b, c, d, deltax, and delta y to perform amendment of the scale factor of a shot revolution, X, and the direction of Y, a shot failure component, and offset here, and Xi and Yi show the image quantity of x directions and the direction of y, respectively.

[0050] next, the difference of the integration imprint distortion data 53 by which shot amendment was carried out in the 1st process, and the integration imprint distortion data 52 in the 2nd process -- data 54 are computed. next, difference -- the correction value A, B, C, D, delta X, and delta Y from which the square sum err of data becomes min is computed.

[0051]

[Equation 11]

$$err = \sum_i \left[\{A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta X - X_i\}^2 + \{A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta Y - Y_i\}^2 \right]$$

$$\cdots (数11)$$

[0052] here -- deltazetaxi and deltazetayi -- difference -- it is data. The strange correction value A, B, C, and D carries out the partial differential of the err by A, B, C, D, delta X, and delta Y, and four simultaneous equations which set each with 0 are obtained by solution Lycium chinense. Thus, the residue data 55 after the computed correction value A, B, C, and D and amendment are registered into the combination information storage means 66 of below-mentioned drawing 10 . In addition, the residue (delta dxi, delta dyi) to each image quantity (Xi, Yi) in the residue data 55 is computed by

the degree type.

[0053]

[Equation 12]

$$\Delta dx_i = A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta X - X_i \quad \cdots \text{(数12)}$$

[0054]

[Equation 13]

$$\Delta dy_i = C(X_i + \Delta\xi x_i) + D(Y_i + \Delta\xi y_i) + \Delta Y - Y_i \quad \cdots \text{(数13)}$$

[0055] Here, the scale factors Mx and My of correction value A, B, C, and D, the shot revolution theta, the direction of X, and the direction of Y and the relation of the shot failure component alpha are given by the bottom formula.

[0056]

[Equation 14]

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} Mx & 0 \\ 0 & My \end{pmatrix} \begin{pmatrix} 1 & \tan\alpha \\ 0 & 1 \end{pmatrix} \quad \cdots \text{(式14)}$$

[0057] Next, the processing flow for utilizing two or more aligners which are another examples of this invention is explained using drawing 3 .

[0058] First, the reticle and the exposure device name which were used at the 1st process which is a substrate layer are searched with step 9100. Next, the distortion data based on the drawing error of the reticle in the 1st process are read at step 9101 from the searched reticle name. Next, the lens distortion data of the aligner in the 1st process are read from the searched exposure device name at step 9102. Furthermore, the distortion data of a wave aberration reason of the aligner in the 1st process are read at step 9103. Moreover, at step 9104, the correction value set as the aligner of the 1st process is read. Correction value is the scale factor of the reticle scanning direction in the imprint image for example, at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image here. Next, the integration imprint distortion of the 1st process is computed by adding the distortion, lens distortion, and wave aberration reason distortion by the reticle drawing error in the 1st process, and amending this with the above-mentioned correction value by step 9105.

[0059] Next, the equipment number machine variable N is set to 0 by step 9200, and the distortion data based on the reticle drawing error of the 2nd process are read at step 9201. Next, the equipment variable N is added one time at step 9301, the lens distortion data of N number machine are read in step 9302, and the wave aberration reason distortion data of the aligner of N number machine in the 2nd process are read at step 9303. Next, the integration imprint distortion of the 2nd process in N number machine is computed by adding each data of distortion by the reticle drawing error in the 2nd process, the lens distortion of N number machine, and the wave aberration reason distortion of N number machine by step 9205.

[0060] Next, by step 9306, the difference of the integration imprint distortion in the 2nd process of the 1st computed at steps 9105 and 9205 and N number machine is computed, and the correction value of the aligner in the 2nd process for amending difference at step 9307 is computed. the location gap after amendment according to this correction value at step 9408 -- the maximum of difference is computed and it compares with the value of standard set up beforehand. the location gap after amendment -- when difference is larger than a value of standard, it judges that N number machine is unsuitable as an aligner of the 2nd process, it returns to step 9301, and the adoption propriety judging of another number machine is processed. the location gap after amendment -- when difference is smaller than a value of standard, it judges that N number machine is proper as an aligner of the 2nd process, and N number machine name and correction value are registered into a storage at step 9409. It considers at step 9411 whether the value of N reached maximum at step 9410 as processing termination noting that the adoption propriety judging of all the target number machines finishes, when it judged and reaches. At step 9410, when the value of N is in transit to maximum, the adoption propriety judging of return and another number machine is performed to step 9301.

[0061] Thus, the resist which carried in to the aligner of the 1st process the semi-conductor wafer which applied the resist to the front face, and was applied to this semi-conductor wafer front face using the 1st mask where correction value is inputted into N number machine selected as an aligner of the 2nd process is exposed, and the 1st circuit pattern is imprinted. The 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 1st circuit pattern at the development process, and carried out the

exposure imprint of the 1st circuit pattern, and was developed at the etching process after that.
[0062] Then, after forming an insulator layer on the 1st circuit pattern formed in this semi-conductor wafer and applying a resist to a front face, it carries in to N number machine selected as an aligner of the 2nd process, and the resist applied to this semi-conductor wafer front face using the 2nd mask is exposed, and the 2nd circuit pattern is imprinted. The 2nd circuit pattern electrically connected to the 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 2nd circuit pattern at the development process, and carried out the exposure imprint of the 2nd circuit pattern, and was developed at the etching process after that.
[0063] Next, drawing 4 explains a parameter required for calculation of wave aberration reason distortion. First, in order to perform image count of the target circuit pattern, the wave aberration 300 of the lighting conditions 2000, the circuit pattern 200, and the exposure lens 30 is needed. About the approach of image count using these parameters, it is indicated by above-mentioned 'Y.Yoshitake et al, SPIE Vol.1463, pp 678-679, and 1991', for example.
[0064] Here, the example of the lighting conditions 2000 by drawing 5 is explained. Drawing 5 (a) is common lighting and can be expressed with the diameter D1 of the lighting light source image 2010, and the diameter Dep of image 31' of the drawing 31 of the exposure lens 30 as a parameter. When it has topology as a circuit pattern 200 in addition to monochrome information, drawing 5 (b) is lighting conditions used when using the so-called phase shift reticle, and its ratio of the diameter D2 of a lighting light source image to Dep is small compared with drawing 5 (a). Drawing 5 (c) is called zona-orbicularis lighting, and can be expressed with the outer diameter D4 and bores D3 and Dep of the lighting light source image 2030.
[0065] Next, drawing 6 explains the example of the circuit pattern 200 of drawing 4 . First, drawing 6 (a) is a line & tooth-space pattern, and consists of area pellucida 202 and the protection-from-light section 202. It can express with the width of face L1 of a line and the pitch P1 of a line & tooth space which are the protection-from-light section 202 as a parameter of a line & tooth-space pattern. Moreover, drawing 6 (b) is the example of a hole pattern, and consists of the protection-from-light section 204 and opening 203. It can express as the aperture width Sy and the pitch Py of the aperture width Sx of x directions, a pitch Px, and the direction of y.
[0066] Next, the example of the wave aberration 300 of drawing 4 is shown. Wave aberration 301 is the example of comatic aberration unsymmetrical in x directions, and is three-dimension-data. Wave aberration 301 is measurable for every image quantity of an exposure lens by the approach of a publication to 'N.R.Farrar et al, SPIE Vol.4000, pp 19-22, and 2000'.
[0067] Here, drawing 8 explains the calculation approach of the wave aberration reason distortion 41 of drawing 2 . As for the optical intensity distribution 2021 of the circuit pattern of drawing 6 (a), the optical reinforcement 0 and the transparency section 201 change [the protection-from-light section 202] between the optical reinforcement 1. If image count is performed by the above-mentioned approach by considering the lighting 2020 shown in the optical intensity distribution 2021 and drawing 5 (a) of a circuit pattern, and wave aberration 301 unsymmetrical in the x directions of drawing 7 as an input, the **** intensity distribution 2022 shown in drawing 8 will be acquired. The image intensity distribution 2022 shift only delta X to the optical intensity distribution 2021 of a circuit pattern for the unsymmetrical wave aberration 301.
[0068] Here, the calculation approach of shift deltaX is explained. When the formula which expresses F (x) and the image intensity distribution 2022 for the formula showing the optical intensity distribution 2021 of a circuit pattern is set to G (x), those convolution integrals H (tau) are [0069].
[Equation 15]

$$H(\tau) = \int F(x)G(\tau - x)dx \qquad \cdots (式15)$$

[0070] It becomes. Here, tau is the shift amount of image intensity-distribution G (x). H (tau) is considered tau To be in a condition without an image shift in the time of whenever [with F (x) when shifting / inequality] being shown, and the time of H (tau) being min being most in agreement in G (X). The value of tau which gives the minimum value of H (tau) like drawing 9 serves as image shift deltaX of drawing 8 . Since the wave aberration 301 of drawing 7 changes with image quantities, the wave aberration reason distortion 41 of drawing 2 is obtained by computing image shift deltaX in each image quantity.
[0071] Next, drawing 10 explains 1 operation gestalt of a semiconductor device manufacturing system. Here, the history information on the identifier of the reticle first used for exposing the exposed substrate 4 illustrated to drawing 4 in the 1st process, lighting conditions, an exposure device identification child, and input correction value is memorized by the history storage means 61 from the aligner 3 with the host computer 6.

[0072] In the 2nd process, a host computer 6 performs the 2nd aligner candidate and correction value of a process first, and the history storage means 61 asks the control means 76 of a control section 7 first.
[0073] A control means 76 searches the combination information storage means 66, and investigates whether there was any combination of the reticle in the 1st process, lighting conditions, an aligner, and the reticle in the 2nd target process this time, lighting conditions and an aligner in the past.
[0074] When there is nothing in the past, the wave aberration reason distortion calculation means 71 acquires the information of the reticle identifier of the 1st process, lighting conditions, and an exposure device identification child from the history storage means 61 first. The information in connection with circuit patterns, such as distortion, line breadth, a pitch, etc. by the reticle drawing error acquired as a result of the wave aberration reason distortion calculation means' 71 searching a reticle data storage means from a reticle identifier, The wave aberration data obtained as a result of searching the wave aberration data storage means 64 by the exposure device identification child, The wave aberration reason distortion data which performed image count and count of an image shift amount from the input parameter, and were obtained as a result in the lighting conditions furthermore acquired from the history storage means 61 are memorized for the wave aberration reason distortion storage means 65 with an exposure device identification child, a reticle identifier, and lighting conditions.
[0075] An integration imprint distortion calculation means next, from a reticle identifier, an exposure device identification child, and lighting conditions The reticle data storage means 62, the lens distortion storage means 63, and the wave aberration reason distortion storage means 65 are searched. Reticle drawing error reason distortion, lens distortion, and wave aberration reason distortion are acquired, and the integration imprint distortion of the 1st process is computed from these, and with a reticle identifier, an exposure device identification child, and lighting conditions, the integration imprint distortion of the 1st process is combined, and it memorizes for the information storage means 66.
[0076] Next, also about the 2nd process, the same processing as the 1st above-mentioned process is performed, the integration imprint distortion of the 2nd process is combined, and it memorizes for the information storage means 66.
[0077] Then, the integration imprint distortion of the 1st process and the 2nd process which the correction value calculation means 73 read from the combination information storage means 66, And the correction value in the 2nd process which makes the difference of integration imprint distortion min from the correction value in the 1st process acquired from the history storage means 61, The difference of the integration imprint distortion at the time of using this correction value is combined, and it memorizes for the information storage means 66 with the correction value of a reticle identifier, an exposure device identification child and lighting conditions, and the 1st process.
[0078] The aligner candidate selection means 74 Next, the aligner of the combination information storage means 66 to the 1st process, The 2nd aligner candidate and reticle of a process to reticle and lighting conditions, From the difference of integration imprint distortion of lighting conditions, maximum is computed, for example, the doubling specification in the 2nd process read from the specification storage means 67 together with this is compared, maximum doubles, and the aligner candidate in the case of being smaller than specification and the difference of integration imprint distortion are sent to the commencement-of-work equipment decision means 75.
[0079] The system operating status of two or more aligner candidates who fulfill the doubling specification of the 2nd process is asked to the system-operating-status storage means 68, and among vacant aligners, the commencement-of-work equipment decision means 75 gives priority to what has the small difference of integration imprint distortion of the 1st process and the 2nd process, it chooses and sends the correction value in the selected identifier and the 2nd selected process of an aligner to a host computer 6.
[0080] A host computer 6 gives exposure in the 2nd process to the exposed substrate illustrated by drawing 4 by sending to the aligner 3 which the aligner which should start construction work was chosen [aligner] based on this information, and had the correction value of the 2nd process chosen.
[0081] In addition, when a control means 76 combines the data of corresponding integration imprint distortion to an inquiry of a host computer and it is found for the information storage means 66, the computation of the corresponding part can be omitted.
[0082]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
(1) In the 2nd process, since it becomes possible to choose the equipment which is vacant out of two or more aligners with which are satisfied of the specification of doubling, an equipment operating ratio can be raised.
(2) Since wave aberration reason distortion is computed not as a fixed value but as a value depending on lighting conditions and a circuit pattern dimension, the data of the wave aberration reason distortion near a more nearly actual value can be obtained.

(3) it carries out about a specific aligner, reticle, lighting conditions, and a circuit pattern dimension -- having -- every combination of said specific conditions -- the location gap after correction value and amendment -- computing the value of difference beforehand -- the location gap after correction value and amendment -- since the calculation time amount of the value of difference is omissible, it becomes possible to acquire the combination of the aligner which fulfills doubling specification, and corresponding correction value at a high speed.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the manufacture approach of the semiconductor device which makes it possible to reduce generating of the doubling gap with a lower layer pattern in an exposure process, and to expose the upper pattern about the manufacture approach of a semiconductor device, and its system.

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PRIOR ART

[Description of the Prior Art] Manufacture of a semiconductor device is performed by etching the film by repeating the process of generating a circuit pattern on a semi-conductor wafer, on each class, after forming the electric conduction film or an insulator layer on a semi-conductor wafer, exposing to a resist the resist which is a sensitization agent and developing the circuit pattern on spreading and reticle on this. At this time, to a substrate layer pattern, if there is a location gap of the circuit pattern at the time of exposure, a circuit will disconnect or short-circuit and will serve as a defect of a semiconductor device. For this reason, an aligner detects optically the alignment mark which is in the periphery of a circuit pattern in advance of exposure of a circuit pattern, and is performing alignment of a substrate layer and an exposure layer by amending measurement and an imprint location for the location of a substrate layer. Since distortion of a projection lens differs between equipment when an aligner which is different in a substrate layer and an exposure layer is used at this time, even if it performs alignment in an alignment mark location, it doubles in the circuit pattern section and a gap arises. For this reason, at the exposure process, the commencement-of-work method (No. limited commencement of work) using the same aligner is always adopted from the first process to the final process. [0003] However, this is a big cause which the operating ratio of an expensive aligner does not go up, and some policies for utilizing two or more aligners between processes are indicated. For example, there is the approach of amending the lens distortion between 2 equipment for a scale factor as indicated by the publication-number No. 92609 [nine to] official report. Moreover, the approach of judging from the difference of the lens distortion between 2 equipments is indicated [whether construction work can be started in a provisional-publication-of-a-patent No. 114132 / 2000 to / official report with Aligner B to the wafer which started construction work with Aligner A, and]. Moreover, the approach of amending the drawing error of reticle by the scale factor of an aligner, a revolution, and perpendicularity control of the stage at the time of scan exposure is indicated by the provisional-publication-of-a-patent No. 124125 [2000 to] official report.

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EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
(1) In the 2nd process, since it becomes possible to choose the equipment which is vacant out of two or more aligners with which are satisfied of the specification of doubling, an equipment operating ratio can be raised.
(2) Since wave aberration reason distortion is computed not as a fixed value but as a value depending on lighting conditions and a circuit pattern dimension, the data of the wave aberration reason distortion near a more nearly actual value can be obtained.
(3) it carries out about a specific aligner, reticle, lighting conditions, and a circuit pattern dimension -- having -- every combination of said specific conditions -- the location gap after correction value and amendment -- computing the value of difference beforehand -- the location gap after correction value and amendment -- since the calculation time amount of the value of difference is omissible, it becomes possible to acquire the combination of the aligner which fulfills doubling specification, and corresponding correction value at a high speed.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] There are the following troubles about the above-mentioned well-known technique. That is, the consideration to wave optics-distortion has fallen out in the above-mentioned example. About lens distortion, there are geometrical optics-distortion and wave optics-distortion of aberration reasons of a lens, such as comatic aberration. Drawing 11 explains the latter.
[0005] The exposure lens 30 has comatic aberration 300 as wave aberration. This is the unsymmetrical aberration resulting from the profile irregularity error of the eccentricity of the element lens for example, at the time of exposure lens 30 assembly, a tilt, and a lens side. on the occasion of exposure, it is shown in drawing 11 (a) -- usually -- everything but lighting -- "-- the number for optical alliance January, 1998 -- zona-orbicularis lighting which is indicated by 4th page" may be applied Exposure with zona-orbicularis lighting is shown in drawing 11 (b). With zona-orbicularis lighting, the cross section of the illumination-light bundle 2002 is the zona orbicularis-like, and it is effective in raising the contrast of an imprint pattern.
[0006] Comatic aberration 300 is as large as the circumference of the exposure lens 30. Therefore, imprint pattern location gap deltaX' of the zona-orbicularis lighting with which the flux of light spreads on the outskirts as shown in drawing 11 usually becomes larger than location gap deltaX in lighting. That is, a location gap of an imprint pattern changes according to the intensity distribution of the flux of light which passes along the exposure lens 30. Moreover, since the locations of the diffracted light which passes along the inside of the exposure lens 30 with the spatial frequency of an imprint pattern but where an illumination-light bundle is the same differ, the amounts of location gaps differ. Drawing 12 shows the case where the exposure light 2003 carries out incidence to a coarse pattern 210 and the coarse detailed pattern 220. Since it passes along the circumference of the exposure lens 30 compared with the case where the direction of the diffracted light 2005 of the detailed pattern 220 with the large angle of diffraction of (b) is the coarse pattern 210 of (a), it becomes larger than amount of location gaps deltax' of (b) rather than amount of location gaps deltax' of (a).
[0007] In order for a location gap of wave optics-distortion, i.e., a wave aberration reason, to change with lighting conditions and imprint pattern sizes from the above thing, it is necessary to compute the magnitude of wave aberration, and lighting conditions and imprint pattern size as a parameter.
[0008] Moreover, according to the direction [each point / image surface top] of distortion, lens distortion which is an above-mentioned wave optics-distortion and geometrical optics-distortion, and the distortion by the reticle drawing error increase at a certain point, and are reduced at a certain point. Therefore, the distortion of the imprint image obtained these results is obtained by adding each distortion two-dimensional. Only one of three distortion is taken into consideration, or the concept [distortion / by two-dimensional addition / integrative] of handling has escaped from the above-mentioned well-known example.
[0009] The object of this invention is giving the manufacture approach of a semiconductor device of performing number machine limited relaxation of an aligner by performing amendment in consideration of an integrative two-dimensional distortion which consists of the above-mentioned geometric lens distortion, wave optics-distortion of a wave aberration reason, and distortion by the reticle drawing error. The new description of this invention will become clear from description and the accompanying drawing of this description.

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MEANS

[Means for Solving the Problem] In order to attain the above-mentioned object, in this invention, in the 1st exposure process, expose a substrate by the 1st circuit pattern, and the 1st circuit pattern is formed on this substrate. In the manufacture approach of the semiconductor device which forms the 2nd circuit pattern which exposes the substrate which formed the 1st circuit pattern in the 2nd exposure process by the 2nd circuit pattern, and is electrically connected to the 1st circuit pattern It asks for the comprehensive imprint-ized distortion of the 1st when exposing a substrate by the 1st circuit pattern in the 1st exposure process. It asks for the comprehensive imprint-ized distortion of the 2nd when exposing a substrate by the 2nd circuit pattern in the 2nd exposure process. The correction value of the 2nd exposure process is calculated based on the comprehensive imprint-ized distortion of the 1st, and the comprehensive imprint-ized distortion of the 2nd. On the 1st circuit pattern formed through the 1st exposure process in the 2nd exposure process amended with this correction value, the 2nd circuit pattern is exposed and the 2nd circuit pattern was formed.
[0011] In order to attain the above-mentioned object, moreover, in this invention The process which applies the 1st resist to a substrate front face in the manufacture approach of a semiconductor device, The 1st exposure process which carries out the exposure imprint of the 1st circuit pattern at the 1st resist applied on the substrate using the 1st aligner, The process which carries out etching processing of the substrate which carried out the exposure imprint of this 1st circuit pattern, and forms the 1st circuit pattern, The process which forms an insulator layer in the substrate in which the 1st circuit pattern was formed, and the process which applies the 2nd resist on a substrate, The 2nd exposure process which carries out the exposure imprint of the 2nd circuit pattern at the 2nd resist applied on the substrate using the 2nd aligner, It sets at the 2nd exposure process including the process which carries out etching processing of the substrate which carried out the exposure imprint of the 2nd circuit pattern, and forms the 2nd circuit pattern. Where amendment based on a reticle drawing error and lens distortion of as opposed to the 1st aligner for the 2nd aligner, and distortion of a wave aberration reason is performed, the 2nd circuit pattern was exposed.
[0012] In order to attain the above-mentioned object, moreover, in this invention In the manufacture approach of the semiconductor device which exposes the circuit pattern of the 2nd process on the circuit pattern of the 1st process (1) The step which reads distortion by the reticle drawing error of said 1st process, (2) The step which reads the lens distortion in the aligner of said 1st process, (3) The step which reads the wave aberration reason distortion in the aligner of said 1st process, (4) The step which reads the correction value set up with the aligner of said 1st process, (5) -- the step which computes distortion by which said 1st process was integrated, and (6) -- with the step which reads distortion by the reticle drawing error of said 2nd process (7) The step which reads the lens distortion in the aligner of said 2nd process, (8) The step which reads the wave aberration reason distortion in the aligner of said 2nd process, (9) -- the step which computes the integration imprint distortion of said 2nd process, and (10) -- with the step which computes that of the difference of the integration imprint distortion of said 2nd process, and the integration imprint distortion of said 1st process (11) It is characterized by having the step which computes the correction value in the aligner of said 2nd process which makes said difference min.
[0013] Since the difference of a near imprint distortion is actually computable by this between two aligners which unified a reticle drawing error, lens distortion, and distortion of a wave aberration reason, it becomes possible to compute correction value with a high precision in the 2nd aligner.
[0014] moreover -- as the manufacture approach of a semiconductor device into which the above was developed -- (12) -- with the step which searches the identifier of reticle and the identifier of an aligner which were used at said 1st process (13) The step which reads distortion by the drawing error of the reticle used at said 1st process, (14) The step which reads the lens distortion in the aligner used at said 1st process, (15) The step which reads the wave aberration reason distortion in the aligner used at said 1st process, (16) The step which reads the correction value at the time of exposure of the aligner used at said 1st process, (17) The step which computes the imprint distortion by the 1st process

from the data of (16) from said step (12), (18) The step which reads distortion by the drawing error of the reticle in said 2nd process, (19) The step which reads the lens distortion of an aligner candidate in said 2nd process, (20) The step which reads the wave aberration reason distortion of an aligner candidate in said 2nd process, (21) The step which computes the integration imprint distortion by the 2nd process from the data of said step (18), (19), and (20), (22) The step which computes the difference of integration imprint distortion in the integration imprint distortion and said 2nd process in said 1st process, (23) -- the location gap after the correction value which makes difference of said integration imprint distortion min, and amendment -- with the step which computes the maximum of difference The maximum of difference is compared with the value of standard set up beforehand. (24) -- the location gap after said amendment -- When smaller than a value of standard, they are recorded or outputted, using said aligner candidate and said correction value as data, and when larger than a value of standard, it is characterized by having the step which chooses the aligner candidate according to return as a step (19).

[0015] Since this becomes possible in the 2nd process to choose the equipment which is vacant out of two or more aligners with which are satisfied of the specification of doubling, an equipment operating ratio can be raised.

[0016] Furthermore, the step which reads distortion of the wave aberration reason of the aligner in the 1st process and 2nd process (25) The step which reads the lighting conditions of this aligner, and the step which reads the dimension information on the circuit pattern on (26) reticles, (27) -- the step which reads the wave aberration for every image quantity of this aligner, and (28) -- with said lighting conditions, said dimension information, and the step that computes the image of said circuit pattern from the wave aberration for said every image quantity (29) It is characterized by having the step which computes distortion of a wave aberration reason from a location gap of the image of said circuit pattern.

[0017] Since this computes wave aberration reason distortion not as a fixed value but as a value depending on lighting conditions and a circuit pattern dimension, the data of the wave aberration reason distortion near a more nearly actual value can be obtained.

[0018] and in the manufacture approach of the above-mentioned semiconductor device, step (13) - (23) and step (25) - (29) carries out about a specific aligner, reticle, lighting conditions, and a circuit pattern dimension -- having -- every combination of specific conditions -- the location gap after correction value and amendment -- the value of difference is computed beforehand and stored in the storage.

[0019] thereby -- the location gap after correction value and amendment -- since the calculation time amount of the value of difference is omissible, it becomes possible to acquire the combination of the aligner which fulfills doubling specification, and corresponding correction value at a high speed.

[0020] In order to attain the above-mentioned object, moreover, in this invention A history storage means to memorize the aligner and the lighting conditions of having used for manufacture of an exposed substrate the semiconductor device manufacturing system which exposes the circuit pattern of the 2nd process on the circuit pattern of the 1st process, correction value, and the history of reticle, A reticle data storage means to memorize the drawing error reason distortion for every reticle, and a typical circuit pattern dimension, A lens distortion storage means to memorize the lens distortion for every aligner, and a wave aberration data storage means to memorize every aligner and the wave aberration data for every image quantity, A wave aberration reason distortion calculation means to compute wave aberration reason distortion from the wave aberration for every said lighting condition, said circuit pattern dimension, and said image quantity, A wave aberration reason distortion storage means to memorize said wave aberration reason distortion, and an integration imprint distortion calculation means to compute integration imprint distortion from said reticle data, said lens distortion data, and said wave aberration data, the difference of two integration imprint distortion -- computing -- this -- with a correction value calculation means to compute the correction value which makes difference min A combination information storage means to memorize a doubling specification storage means to memorize a product and the doubling specification for every process, said two aligners, said lighting conditions, the information on said reticle, corresponding correction value, and integration imprint distortion maximum, The history information about the 1st process corresponding to said exposed substrate is read from a history storage means. The aligner of this history information, lighting conditions, the aligner of the 2nd process corresponding to reticle, By comparing the difference of said integration imprint distortion corresponding to lighting conditions, and the doubling specification and the 1st process corresponding to the 2nd process for a candidate, and the 2nd process of reticle A commencement-of-work decision means to have compared with the system operating status of a actual aligner the aligner which can start construction work, lighting conditions, a candidate selection means to choose the candidate of reticle, and the candidate of the aligner, in which said commencement of work is possible, and to judge the aligner which starts construction work was had and constituted.

[0021] Thereby, acquisition of the correction value between 2 equipments by integration imprint distortion and selection

of the aligner in consideration of doubling specification which can be started can carry out efficiently.
[0022]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing. A processing flow for drawing 1 to compute the correction value of the aligner in the semiconductor device production process which is 1 operation gestalt of this invention, and drawing 2 show the mimetic diagram of the target two-dimensional-in processing flow distortion data. First, the processing flow for computing the correction value of an aligner by drawing 1 is explained.
[0023] First, the distortion data based on the drawing error of the reticle in the 1st process are read at step 9101. Next, the lens distortion data of the aligner in the 1st process are read at step 9102. Furthermore, the distortion data of a wave aberration reason of the aligner in the 1st process are read at step 9103. Moreover, at step 9104, the correction value set as the aligner of the 1st process is read. Correction value is the scale factor of the reticle scanning direction in the imprint image for example, at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image here. Next, the integration imprint distortion of the 1st process is computed by adding the distortion, lens distortion, and wave aberration reason distortion by the reticle drawing error in the 1st process, and amending this with the above-mentioned correction value by step 9105.
[0024] Next, in steps 9201-9203, the integration imprint distortion of the 2nd process is computed by reading each data of distortion by the reticle error in the 2nd process, lens distortion, and wave aberration reason distortion, and adding these at step 9205.
[0025] Next, by step 9306, the difference of the integration imprint distortion in the 1st and 2nd processes computed at steps 9105 and 9205 is computed, and the correction value of the aligner in the 2nd process for amending difference at step 9307 is computed. This correction value is the scale factor of the reticle scanning direction in the imprint image at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image like the above.
[0026] Finally in step 9308, this correction value is inputted into the aligner of the 2nd process.
[0027] Thus, the resist which carried in to the aligner of the 1st process the semi-conductor wafer which applied the resist to the front face, and was applied to this semi-conductor wafer front face using the 1st mask where correction value is inputted into the aligner of the 2nd process is exposed, and the 1st circuit pattern is imprinted. The 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 1st circuit pattern at the development process, and carried out the exposure imprint of the 1st circuit pattern, and was developed at the etching process after that.
[0028] Then, after forming an insulator layer on the 1st circuit pattern formed in this semi-conductor wafer and applying a resist to a front face, it carries in to the aligner of the 2nd process, and the resist applied to this semi-conductor wafer front face using the 2nd mask is exposed, and the 2nd circuit pattern is imprinted. The 2nd circuit pattern electrically connected to the 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 2nd circuit pattern at the development process, and carried out the exposure imprint of the 2nd circuit pattern, and was developed at the etching process after that.
[0029] Next, drawing 2 explains each distortion data in the processing flow for computing the correction value of the aligner of drawing 1 . The distortion measure point of the distortion data 21 based on the reticle error of the 1st process is the grid 213 which consisted of reticle marks 211 and 212 of right and left used as the criteria of reticle alignment, and a circuit pattern chosen from the design data. An absolute coordinate is measured by the coordinate measuring device with which these were equipped with the laser length measuring machine etc. The distortion data 21 based on a reticle error consist of what asked for the difference delta Rxi and delta Ryi of the x directions of the coordinate on the design of each circuit pattern obtained when the scale factor of a design-data coordinate and a revolution are amended so that the measurement coordinate of the reticle marks 211 and 212 may be in agreement with the coordinate on a design, and the actually measured coordinate, and the direction of y in each measure point i, and the absolute coordinate itself which measured the reticle marks 211 and 212. The distortion data 22 based on the reticle error of the 2nd process are also obtained in the same procedure as the above.
[0030] The distortion data 31 of the aligner in the 1st process expose the reticle for assessment other than the product reticle of each above-mentioned process in which the pattern arranged on a grid is contained on an exposed substrate, and are obtained by measuring the formed imprint pattern with the above-mentioned coordinate measuring device.

Moreover, although the reticle marks 311 and 312 on reticle are not exposed with the gobo (masking blade) of an aligner, they are usually exposed on an exposed substrate to a pattern and coincidence by this measurement, without shading. The coordinate of the reticle marks 311 and 312 formed in the exposed substrate is also measured, and it includes in the distortion data 31 of the aligner in the 1st process. In case [in which this is based on a reticle error later] distortion of an aligner is added distorted, it is used for carrying out alignment of both distorted data.
[0031] Here, how to ask for the distortion data 31 of an aligner from the measurement coordinate of the imprint pattern arranged on the grid of the above-mentioned reticle for assessment is explained. For that, amendment first needs to remove position error deltaSrxi of the x directions of each pattern of a drawing error reason of the reticle for distortion measurement assessment, and the direction of y, and deltaSryi. i corresponds to Pattern i. deltaSrxi and deltaSryi are obtained by "the-one number" and "a-two number."
[0032]
[Equation 1]
$$\Delta Srx_i = Srx_i - Sdx_i \quad \cdots (数1)$$

[0033]
[Equation 2]
$$\Delta Sry_i = Sry_i - Sdy_i \quad \cdots (数2)$$

[0034] The absolute-measurement coordinate of the x directions of each pattern [in / here / in Srxi and Sryi / the reticle for assessment] i and the direction of y, Sdxi, and Sdyi are the design value coordinates of the x directions of each pattern i in the reticle for assessment, and the direction of y. On the other hand, distortion data deltaSlenxi of the aligner in the 1st process and deltaSlenyi are obtained by "the-three number" and "a-four number."
[0035]
[Equation 3]
$$\Delta Slenx_i = Smx_i - Srx_i \quad \cdots (数3)$$

[0036]
[Equation 4]
$$\Delta Sleny_i = Smy_i - Sry_i \quad \cdots (数4)$$

[0037] Smxi and Smyi are the measured value of the absolute coordinate of an imprint pattern [in / here / an exposed substrate]. therefore, "a-one number", "a-two number", "a-three number", and "a-four number" -- deltaSlenxi and deltaSlenyi -- [0038]
[Equation 5]
$$\Delta Slenx_i = Smx_i - Sdx_i + \Delta Srx_i \quad \cdots (数5)$$

[0039]
[Equation 6]
$$\Delta Sleny_i = Smy_i - Sdy_i + \Delta Sry_i \quad \cdots (数6)$$

[0040] It becomes. The distorted data 31 of the aligner in the 1st process are obtained by these actuation. The distorted data 32 of the aligner in the 2nd process are also obtained by same actuation.
[0041] Next, how to ask for the wave aberration reason distortion data 41 of the aligner in the 1st process is explained. The above-mentioned distortion data 31 base [geometrical optics-distortion is shown and] on the magnitude and the lighting conditions of a pattern and are fixed. However, intensity distribution are in the imprint diffracted light according to the magnitude and the lighting conditions of a pattern in wave optics. Since the weight of the passage location in an exposure lens differs, the deflection from the distorted data 31 of the aligner which is geometrical optics-distortion arises in an imprint location by wave aberration. It is the distortion data 41 of a wave aberration reason which showed this deflection.
[0042] As drawing 5 and drawing 6 were quoted and explained previously, the distortion of a wave aberration reason is dependent on the spatial frequency of wave aberration and lighting conditions, or a pattern. Then, by inputting measurement punishment, this, a reticle pattern, and lighting conditions for the wave aberration 300 for every image quantity of the exposure lens 30 beforehand, it asks for the imprint image on an exposed substrate by wave optics-numerical calculation, and location gap deltaX' is computed. The count approach of an imprint image is 'Y.Yoshitake et al, SPIE Vol.1463, pp 678-679, and 1991'. It is indicated. A location gap is given by computing the difference delta Wxi

and delta Wyi of the center of gravity of the optical intensity distribution of an imprint image, and a reticle pattern-design location for example, in each image quantity i of every. Moreover, when asking for integration imprint distortion by the distorted data 31 of an aligner and the addition of the wave aberration reason distortion 41 which are geometrical optics-distortion, in each image quantity, it asks for a location gap as difference of the core of the optical intensity distribution of an imprint image, and the distorted data 31 of an aligner. In addition, the wave aberration reason distortion data 42 of the aligner in the 2nd process are also obtained by same actuation.

[0043] deltaxixi and deltaxiyi which are the integration imprint distortion data 51 are obtained by the degree type.

[0044]

[Equation 7]

$$\Delta\xi x_i = \Delta Srx_i + \Delta Slenx_i + \Delta Wx_i \quad \cdots (数7)$$

[0045]

[Equation 8]

$$\Delta\xi y_i = \Delta Sry_i + \Delta Sleny_i + \Delta Wy_i \quad \cdots (数8)$$

[0046] The aligner is performing shot amendment of the exposure layer to a substrate layer by rotating an exposed substrate. Moreover, in the case of the scanning aligner, control of the stage in which an exposed substrate is carried is performing the scale factor and shot failure component of a scanning direction. Therefore, delta xi'xi and delta xi'yi which are the integration imprint distortion data 53 which considered the shot correction value of the exposure layer to a substrate layer are [0047].

[Equation 9]

$$\Delta\xi' x_i = a(X_i + \Delta\xi x_i) + b(Y_i + \Delta\xi y_i) + \Delta x - X_i \quad \cdots (数9)$$

[0048]

[Equation 10]

$$\Delta\xi' y_i = c(X_i + \Delta\xi x_i) + d(Y_i + \Delta\xi y_i) + \Delta y - Y_i \quad \cdots (数10)$$

[0049] Correction value for a, b, c, d, deltax, and delta y to perform amendment of the scale factor of a shot revolution, X, and the direction of Y, a shot failure component, and offset here, and Xi and Yi show the image quantity of x directions and the direction of y, respectively.

[0050] next, the difference of the integration imprint distortion data 53 by which shot amendment was carried out in the 1st process, and the integration imprint distortion data 52 in the 2nd process -- data 54 are computed. next, difference -- the correction value A, B, C, D, delta X, and delta Y from which the square sum err of data becomes min is computed.

[0051]

[Equation 11]

$$err = \sum_i \left[\{A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta X - X_i\}^2 + \{A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta Y - Y_i\}^2 \right] \quad \cdots (数11)$$

[0052] here -- deltazetaxi and deltazetayi -- difference -- it is data. The strange correction value A, B, C, and D carries out the partial differential of the err by A, B, C, D, delta X, and delta Y, and four simultaneous equations which set each with 0 are obtained by solution Lycium chinense. Thus, the residue data 55 after the computed correction value A, B, C, and D and amendment are registered into the combination information storage means 66 of below-mentioned drawing 10 . In addition, the residue (delta dxi, delta dyi) to each image quantity (Xi, Yi) in the residue data 55 is computed by the degree type.

[0053]

[Equation 12]

$$\Delta dx_i = A(X_i + \Delta\xi x_i) + B(Y_i + \Delta\xi y_i) + \Delta X - X_i \quad \cdots (数12)$$

[0054]

[Equation 13]

$$\Delta dy_i = C(X_i + \Delta\xi x_i) + D(Y_i + \Delta\xi y_i) + \Delta Y - Y_i \quad \cdots (数13)$$

[0055] Here, the scale factors Mx and My of correction value A, B, C, and D, the shot revolution theta, the direction of X, and the direction of Y and the relation of the shot failure component alpha are given by the bottom formula.

[0056]
[Equation 14]

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} Mx & 0 \\ 0 & My \end{pmatrix} \begin{pmatrix} 1 & \tan\alpha \\ 0 & 1 \end{pmatrix} \quad \cdots (式14)$$

[0057] Next, the processing flow for utilizing two or more aligners which are another examples of this invention is explained using drawing 3 .
[0058] First, the reticle and the exposure device name which were used at the 1st process which is a substrate layer are searched with step 9100. Next, the distortion data based on the drawing error of the reticle in the 1st process are read at step 9101 from the searched reticle name. Next, the lens distortion data of the aligner in the 1st process are read from the searched exposure device name at step 9102. Furthermore, the distortion data of a wave aberration reason of the aligner in the 1st process are read at step 9103. Moreover, at step 9104, the correction value set as the aligner of the 1st process is read. Correction value is the scale factor of the reticle scanning direction in the imprint image for example, at the time of exposure, the scale factor of the direction which intersects perpendicularly with a reticle scanning direction, the perpendicularity of a reticle scanning direction and an exposed substrate scanning direction, and this imprint rotation of image here. Next, the integration imprint distortion of the 1st process is computed by adding the distortion, lens distortion, and wave aberration reason distortion by the reticle drawing error in the 1st process, and amending this with the above-mentioned correction value by step 9105.
[0059] Next, the equipment number machine variable N is set to 0 by step 9200, and the distortion data based on the reticle drawing error of the 2nd process are read at step 9201. Next, the equipment variable N is added one time at step 9301, the lens distortion data of N number machine are read in step 9302, and the wave aberration reason distortion data of the aligner of N number machine in the 2nd process are read at step 9303. Next, the integration imprint distortion of the 2nd process in N number machine is computed by adding each data of distortion by the reticle drawing error in the 2nd process, the lens distortion of N number machine, and the wave aberration reason distortion of N number machine by step 9205.
[0060] Next, by step 9306, the difference of the integration imprint distortion in the 2nd process of the 1st computed at steps 9105 and 9205 and N number machine is computed, and the correction value of the aligner in the 2nd process for amending difference at step 9307 is computed. the location gap after amendment according to this correction value at step 9408 -- the maximum of difference is computed and it compares with the value of standard set up beforehand. the location gap after amendment -- when difference is larger than a value of standard, it judges that N number machine is unsuitable as an aligner of the 2nd process, it returns to step 9301, and the adoption propriety judging of another number machine is processed. the location gap after amendment -- when difference is smaller than a value of standard, it judges that N number machine is proper as an aligner of the 2nd process, and N number machine name and correction value are registered into a storage at step 9409. It considers at step 9411 whether the value of N reached maximum at step 9410 as processing termination noting that the adoption propriety judging of all the target number machines finishes, when it judged and reaches. At step 9410, when the value of N is in transit to maximum, the adoption propriety judging of return and another number machine is performed to step 9301.
[0061] Thus, the resist which carried in to the aligner of the 1st process the semi-conductor wafer which applied the resist to the front face, and was applied to this semi-conductor wafer front face using the 1st mask where correction value is inputted into N number machine selected as an aligner of the 2nd process is exposed, and the 1st circuit pattern is imprinted. The 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 1st circuit pattern at the development process, and carried out the exposure imprint of the 1st circuit pattern, and was developed at the etching process after that.
[0062] Then, after forming an insulator layer on the 1st circuit pattern formed in this semi-conductor wafer and applying a resist to a front face, it carries in to N number machine selected as an aligner of the 2nd process, and the resist applied to this semi-conductor wafer front face using the 2nd mask is exposed, and the 2nd circuit pattern is imprinted. The 2nd circuit pattern electrically connected to the 1st circuit pattern is formed on a semi-conductor wafer by carrying out etching processing of the semi-conductor wafer by using as a mask the resist which developed the resist which processed next the semi-conductor wafer which carried out the exposure imprint of this 2nd circuit pattern at the development process, and carried out the exposure imprint of the 2nd circuit pattern, and was developed at the etching process after that.
[0063] Next, drawing 4 explains a parameter required for calculation of wave aberration reason distortion. First, in order to perform image count of the target circuit pattern, the wave aberration 300 of the lighting conditions 2000, the circuit

pattern 200, and the exposure lens 30 is needed. About the approach of image count using these parameters, it is indicated by above-mentioned 'Y.Yoshitake et al, SPIE Vol.1463, pp 678-679, and 1991', for example.
[0064] Here, the example of the lighting conditions 2000 by drawing 5 is explained. Drawing 5 (a) is common lighting and can be expressed with the diameter D1 of the lighting light source image 2010, and the diameter Dep of image 31' of the drawing 31 of the exposure lens 30 as a parameter. When it has topology as a circuit pattern 200 in addition to monochrome information, drawing 5 (b) is lighting conditions used when using the so-called phase shift reticle, and its ratio of the diameter D2 of a lighting light source image to Dep is small compared with drawing 5 (a). Drawing 5 (c) is called zona-orbicularis lighting, and can be expressed with the outer diameter D4 and bores D3 and Dep of the lighting light source image 2030.
[0065] Next, drawing 6 explains the example of the circuit pattern 200 of drawing 4 . First, drawing 6 (a) is a line & tooth-space pattern, and consists of area pellucida 202 and the protection-from-light section 202. It can express with the width of face L1 of a line and the pitch P1 of a line & tooth space which are the protection-from-light section 202 as a parameter of a line & tooth-space pattern. Moreover, drawing 6 (b) is the example of a hole pattern, and consists of the protection-from-light section 204 and opening 203. It can express as the aperture width Sy and the pitch Py of the aperture width Sx of x directions, a pitch Px, and the direction of y.
[0066] Next, the example of the wave aberration 300 of drawing 4 is shown. Wave aberration 301 is the example of comatic aberration unsymmetrical in x directions, and is three-dimension-data. Wave aberration 301 is measurable for every image quantity of an exposure lens by the approach of a publication to 'N.R.Farrar et al, SPIE Vol.4000, pp 19-22, and 2000'.
[0067] Here, drawing 8 explains the calculation approach of the wave aberration reason distortion 41 of drawing 2 . As for the optical intensity distribution 2021 of the circuit pattern of drawing 6 (a), the optical reinforcement 0 and the transparency section 201 change [the protection-from-light section 202] between the optical reinforcement 1. If image count is performed by the above-mentioned approach by considering the lighting 2020 shown in the optical intensity distribution 2021 and drawing 5 (a) of a circuit pattern, and wave aberration 301 unsymmetrical in the x directions of drawing 7 as an input, the **** intensity distribution 2022 shown in drawing 8 will be acquired. The image intensity distribution 2022 shift only delta X to the optical intensity distribution 2021 of a circuit pattern for the unsymmetrical wave aberration 301.
[0068] Here, the calculation approach of shift deltaX is explained. When the formula which expresses F (x) and the image intensity distribution 2022 for the formula showing the optical intensity distribution 2021 of a circuit pattern is set to G (x), those convolution integrals H (tau) are [0069].
[Equation 15]

$$H(\tau) = \int F(x)G(\tau - x)dx \qquad \cdots (式15)$$

[0070] It becomes. Here, tau is the shift amount of image intensity-distribution G (x). H (tau) is considered tau To be in a condition without an image shift in the time of whenever [with F (x) when shifting / inequality] being shown, and the time of H (tau) being min being most in agreement in G (X). The value of tau which gives the minimum value of H (tau) like drawing 9 serves as image shift deltaX of drawing 8 . Since the wave aberration 301 of drawing 7 changes with image quantities, the wave aberration reason distortion 41 of drawing 2 is obtained by computing image shift deltaX in each image quantity.
[0071] Next, drawing 10 explains 1 operation gestalt of a semiconductor device manufacturing system. Here, the history information on the identifier of the reticle first used for exposing the exposed substrate 4 illustrated to drawing 4 in the 1st process, lighting conditions, an exposure device identification child, and input correction value is memorized by the history storage means 61 from the aligner 3 with the host computer 6.
[0072] In the 2nd process, a host computer 6 performs the 2nd aligner candidate and correction value of a process first, and the history storage means 61 asks the control means 76 of a control section 7 first.
[0073] A control means 76 searches the combination information storage means 66, and investigates whether there was any combination of the reticle in the 1st process, lighting conditions, an aligner, and the reticle in the 2nd target process this time, lighting conditions and an aligner in the past.
[0074] When there is nothing in the past, the wave aberration reason distortion calculation means 71 acquires the information of the reticle identifier of the 1st process, lighting conditions, and an exposure device identification child from the history storage means 61 first. The information in connection with circuit patterns, such as distortion, line breadth, a pitch, etc. by the reticle drawing error acquired as a result of the wave aberration reason distortion calculation means' 71 searching a reticle data storage means from a reticle identifier, The wave aberration data obtained as a result of searching the wave aberration data storage means 64 by the exposure device identification child, The wave aberration

reason distortion data which performed image count and count of an image shift amount from the input parameter, and were obtained as a result in the lighting conditions furthermore acquired from the history storage means 61 are memorized for the wave aberration reason distortion storage means 65 with an exposure device identification child, a reticle identifier, and lighting conditions.

[0075] An integration imprint distortion calculation means next, from a reticle identifier, an exposure device identification child, and lighting conditions The reticle data storage means 62, the lens distortion storage means 63, and the wave aberration reason distortion storage means 65 are searched. Reticle drawing error reason distortion, lens distortion, and wave aberration reason distortion are acquired, and the integration imprint distortion of the 1st process is computed from these, and with a reticle identifier, an exposure device identification child, and lighting conditions, the integration imprint distortion of the 1st process is combined, and it memorizes for the information storage means 66.

[0076] Next, also about the 2nd process, the same processing as the 1st above-mentioned process is performed, the integration imprint distortion of the 2nd process is combined, and it memorizes for the information storage means 66.

[0077] Then, the integration imprint distortion of the 1st process and the 2nd process which the correction value calculation means 73 read from the combination information storage means 66, And the correction value in the 2nd process which makes the difference of integration imprint distortion min from the correction value in the 1st process acquired from the history storage means 61, The difference of the integration imprint distortion at the time of using this correction value is combined, and it memorizes for the information storage means 66 with the correction value of a reticle identifier, an exposure device identification child and lighting conditions, and the 1st process.

[0078] The aligner candidate selection means 74 Next, the aligner of the combination information storage means 66 to the 1st process, The 2nd aligner candidate and reticle of a process to reticle and lighting conditions, From the difference of integration imprint distortion of lighting conditions, maximum is computed, for example, the doubling specification in the 2nd process read from the specification storage means 67 together with this is compared, maximum doubles, and the aligner candidate in the case of being smaller than specification and the difference of integration imprint distortion are sent to the commencement-of-work equipment decision means 75.

[0079] The system operating status of two or more aligner candidates who fulfill the doubling specification of the 2nd process is asked to the system-operating-status storage means 68, and among vacant aligners, the commencement-of-work equipment decision means 75 gives priority to what has the small difference of integration imprint distortion of the 1st process and the 2nd process, it chooses and sends the correction value in the selected identifier and the 2nd selected process of an aligner to a host computer 6.

[0080] A host computer 6 gives exposure in the 2nd process to the exposed substrate illustrated by drawing 4 by sending to the aligner 3 which the aligner which should start construction work was chosen [aligner] based on this information, and had the correction value of the 2nd process chosen.

[0081] In addition, when a control means 76 combines the data of corresponding integration imprint distortion to an inquiry of a host computer and it is found for the information storage means 66, the computation of the corresponding part can be omitted.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is flow drawing explaining the correction value calculation flow of the aligner using the integration imprint distortion by this invention.
[Drawing 2] It is drawing explaining each distortion in the flow of drawing 1 , integration imprint distortion, and the method of computing correction value.
[Drawing 3] It is drawing explaining the flow of correction value calculation of an aligner and the flow of aligner selection in the manufacture approach of the semiconductor device which is another example of this invention.
[Drawing 4] It is the schematic elevation explaining a parameter required for wave aberration reason distortion calculation of optical system.
[Drawing 5] Drawing which explains lighting conditions among the parameters of drawing 4 .
[Drawing 6] Drawing which explains a circuit pattern among the parameters of drawing 4 .
[Drawing 7] Drawing which explains wave aberration among the parameters of drawing 4 .
[Drawing 8] Drawing explaining an image shift.
[Drawing 9] Drawing which carries out [****] and explains the relation of the convolution integral of an amount tau, a circuit pattern light change on the strength, and a **** change on the strength.
[Drawing 10] Drawing explaining the semiconductor device manufacturing system which is another example of this invention.
[Drawing 11] Drawing explaining a lighting configuration and the relation of an image shift.
[Drawing 12] Drawing explaining the relation between a circuit pattern and an image shift.
[Description of Notations]
21 -- Reticle drawing error reason distortion of the 1st process 22 -- Reticle drawing error reason distortion of the 2nd process 31 -- Lens distortion of the aligner of the 1st process 32 -- Lens distortion of the aligner of the 2nd process 41 -- Wave aberration reason distortion of the 1st process 42 -- Wave aberration reason distortion of the 2nd process 51 -- Integration imprint distortion of the 1st process
52 -- Integration imprint distortion of the 2nd process
2000 -- Lighting conditions 200 -- Circuit pattern 300 -- Wave aberration data
2 -- Reticle 31 -- Pupil 30 -- Exposure lens 4 -- Exposed substrate 60 -- Network
61 -- History storage means 62 -- Reticle data storage means 63 -- Lens distortion storage means
64 -- Wave aberration data storage means 65 -- Wave aberration reason distortion storage means 66 -- Combination information storage means 67 -- Doubling specification storage means 68 -- System-operating-status storage means 7 -- Control section 71 -- Wave aberration reason distortion calculation means 72 -- Integration imprint distortion calculation means 73 -- Correction value calculation means 74 -- Aligner candidate calculation means 75 -- Commencement-of-work equipment decision means 6 -- Host computer 3 -- Aligner

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[Translation done.]

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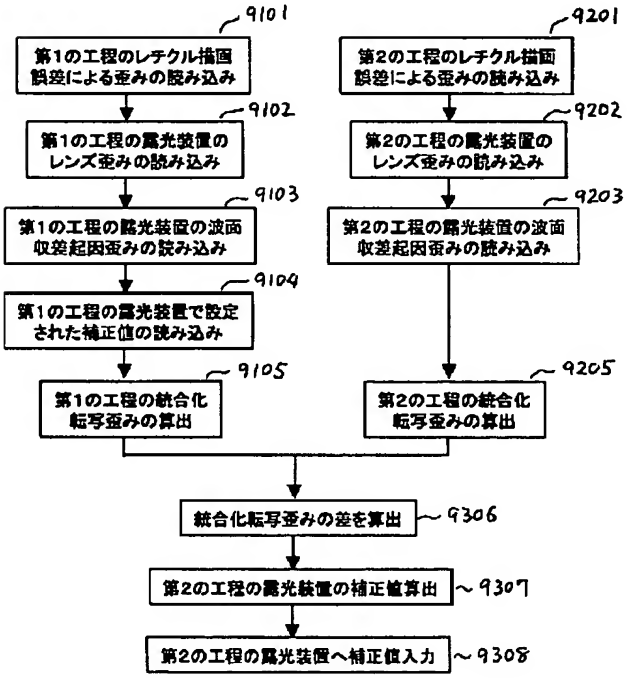
DRAWINGS

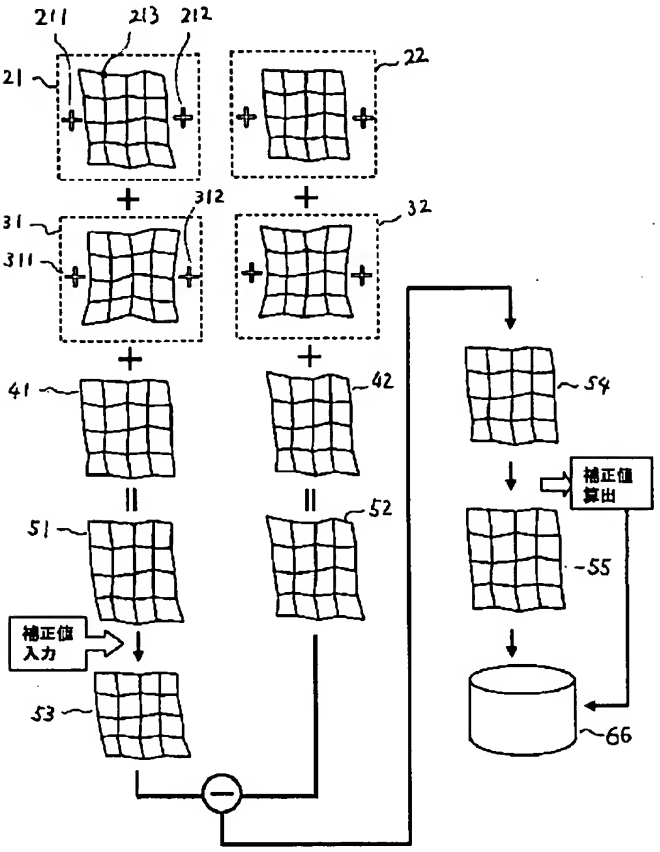
[Drawing 1]

図1



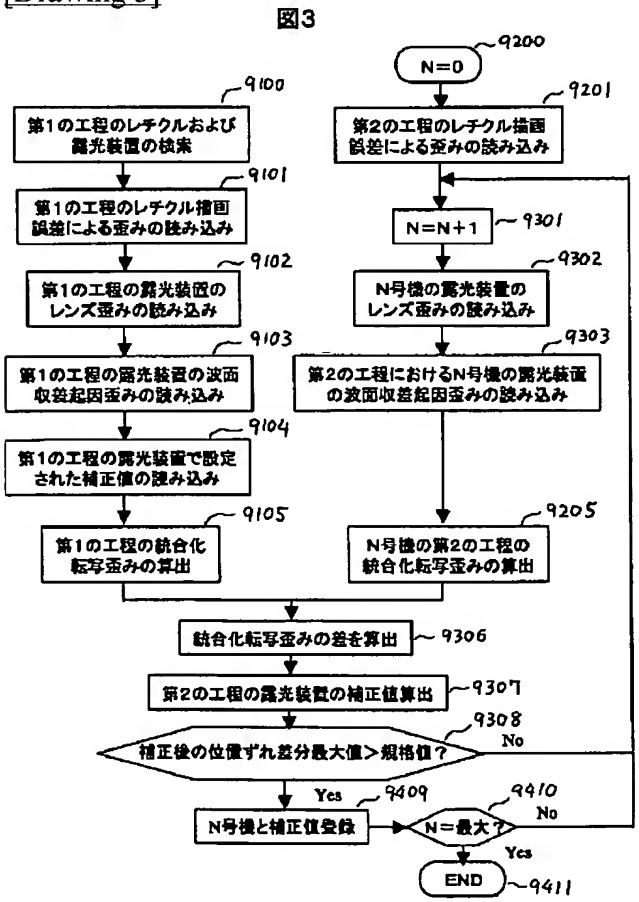
[Drawing 2]

図2



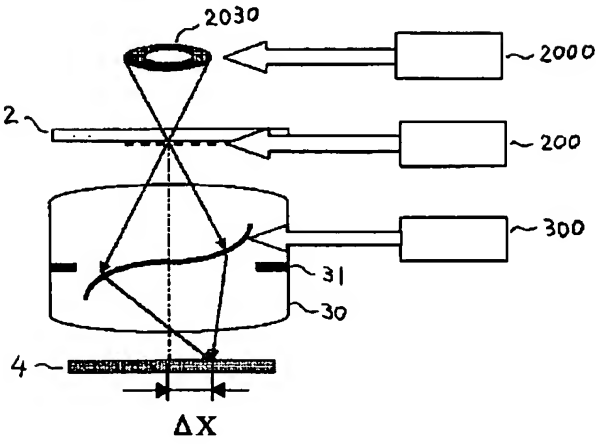
[Drawing 3]

図3



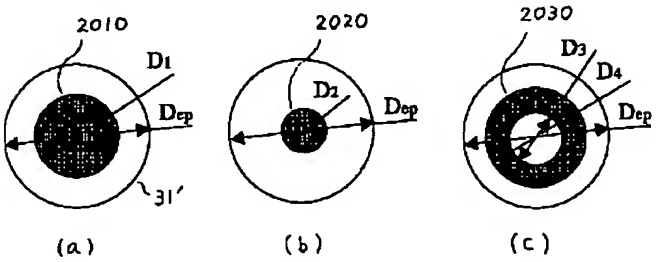
[Drawing 4]

図 4



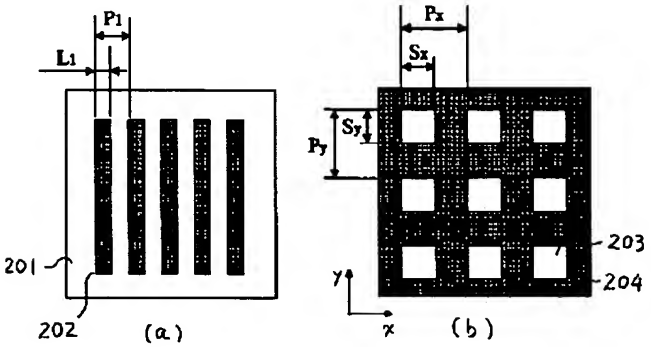
[Drawing 5]

図 5



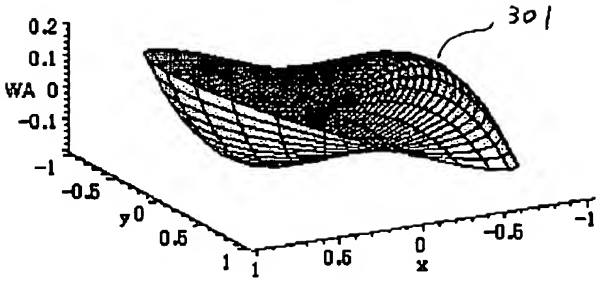
[Drawing 6]

図 6



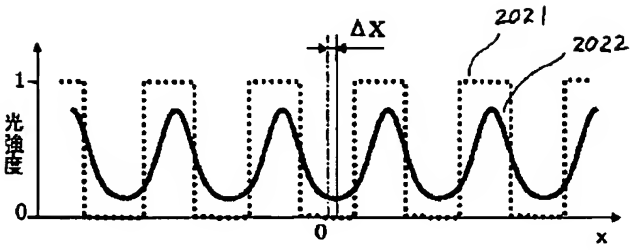
[Drawing 7]

図 7



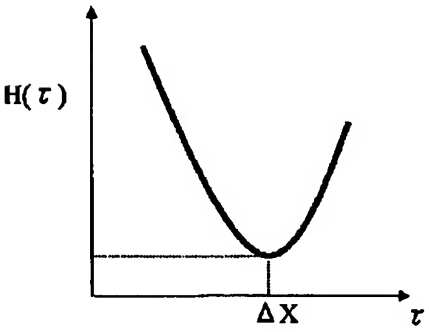
[Drawing 8]

図 8



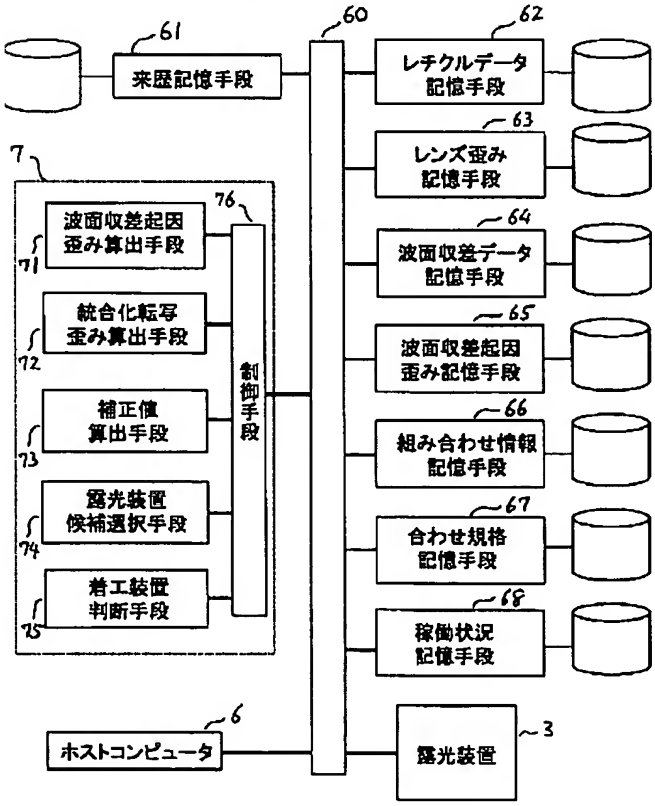
[Drawing 9]

図 9



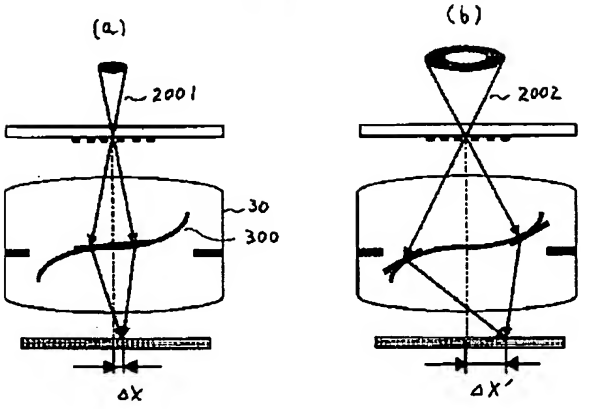
[Drawing 10]

図 10



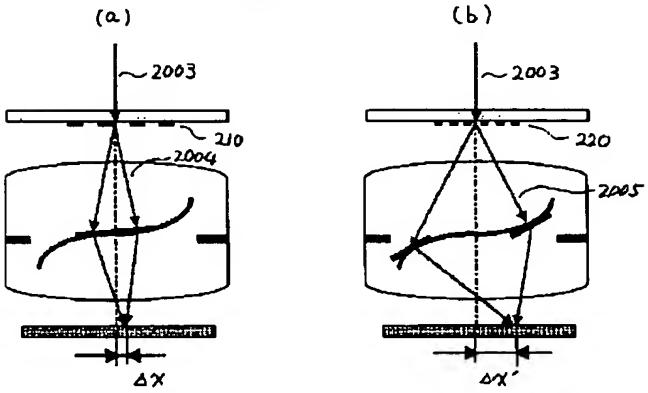
[Drawing 11]

図11



[Drawing 12]

図12



[Translation done.]